decoding information according to a modified Walsh code reducing an average DC signal component which in combination with the AC-coupling to said at least one A/D converter enhances overall performance, and

a modulator for spread spectrum PSK modulating information for transmission via the radio circuit, said modulator comprising at least one modified Walsh code function encoder for encoding information according to the modified Walsh code.

63. A spread spectrum radio transceiver according to claim 62 wherein said modulator is configured to operate in one of first format defined by bi-phase PSK (BPSK) modulation at a first data rate and a second format defined by quadrature PSK (QPSK) modulation at a second data rate; and wherein said demodulator is configured to operate in one of the first and second formats.

64. A spread spectrum radio transceiver according to claim 63 wherein said modulator is configured to modulate data packets to include a header in a third format defined by a predetermined modulation at a third data rate and variable data in one of the first and second formats; and wherein said demodulator is configured to demodulate data packets by demodulating the header in the third format and for switching to the respective one of the first and second formats of the variable data after the header.

65. A spread spectrum radio transceiver according to claim 64 wherein the predetermined modulation of the third format is differential BPSK (DBPSK), and wherein the third data rate is lower than the first and second data rates.

66. A spread spectrum radio transceiver according to claim 64 wherein said demodulator further comprises:

a first carrier tracking loop for the third format; and

a second carrier tracking loop for the first and second formats.

67. A spread spectrum radio transceiver according to claim 66 wherein said second carrier tracking loop comprises:

a carrier numerically controlled oscillator (NCO); and

a controller to selectively operate said carrier NCO based upon a carrier phase of said first carrier tracking loop to thereby facilitate switching to the format of the variable data.

68. A spread spectrum radio transceiver according to claim 66 wherein said second carrier tracking loop comprises:

a carrier loop filter; and

a controller to selectively operate said carrier loop filter based upon a frequency of said first carrier tracking loop to thereby facilitate switching to the format of the variable data.

69. A spread spectrum radio transceiver according to claim 62 wherein said modulator is further configured to partition data into four bit nibbles of sign (one bit) and magnitude (three bits) to said at least one modified Walsh code function encoder.

70. A spread spectrum radio transceiver according to claim 62 wherein the modified Walsh code is a Walsh code modified by a modulo two addition of a fixed hexadecimal code thereto.

71. A spread spectrum radio transceiver according to claim 62 wherein said at least one modified Walsh code function correlator comprises:

a modified Walsh function generator; and

a plurality of parallel connected correlators connected to said modified Walsh function generator.

72. A spread spectrum radio transceiver according to claim 62 wherein said modulator is configured to spread each data bit using a pseudorandom (PN) sequence at a predetermined chip rate and is configured to generate a preamble; and wherein said demodulator is configured to demodulate the preamble for achieving initial PN sequence synchronization.

73. A spread spectrum radio transceiver according to claim 62 wherein said modulator comprises a scrambler; and wherein said demodulator comprises a descrambler.

74. A spread spectrum radio transceiver according to claim 62 wherein said demodulator is configured to generate a clear channel assessment signal.

75. A spread spectrum radio transceiver according to claim 62 wherein said radio circuit comprises:
a quadrature intermediate frequency modulator/demodulator connected to said baseband processor; and
an up/down frequency converter connected to said quadrature intermediate frequency modulator/demodulator.

76. A spread spectrum radio transceiver according to claim 75 wherein said radio circuit further comprises:
a low noise amplifier having an output connected to an input of said up/down converter; and
a radio frequency power amplifier having an input connected to an output of said up/down converter.

77. A spread spectrum radio transceiver according to claim 76 further comprising:
an antenna; and
an antenna switch for switching said antenna between the output of said radio frequency power amplifier and the input of said low noise amplifier.

78. A baseband processor for a spread spectrum radio transceiver, said baseband processor comprising:
a demodulator for spread spectrum phase shift keying (PSK) demodulating;
at least one analog-to-digital (A/D) converter having an output connected to said demodulator and an input AC-coupled to receive information;
said demodulator comprising at least one predetermined orthogonal code function correlator for decoding information according to a predetermined orthogonal code reducing an average DC signal component to thereby increase AC-coupling to said at least one A/D converter; and

a modulator for spread spectrum PSK modulating information for transmission, said modulator comprising at least one predetermined orthogonal code function encoder for encoding information according to the predetermined orthogonal code.

79. A baseband processor according to claim 78 wherein said modulator is configured to operate in one of first format defined by bi-phase PSK (BPSK) modulation at a first data rate and a second format defined by quadrature PSK (QPSK) modulation at a second data rate; and wherein said demodulator is configured to operate in one of the first and second formats.

80. A baseband processor according to claim 79 wherein said modulator is configured to modulate data packets to include a header in a third format defined by a predetermined modulation at a third data rate and variable data in one of the first and second formats; and wherein said demodulator comprises is configured to demodulate data packets by demodulating the header in the third format and for switching to the respective one of the first and second formats of the variable data after the header.

81. A baseband processor according to claim 80 wherein the predetermined modulation of the third format is differential BPSK (DBPSK), and wherein the third data rate is lower than the first and second data rates.

82. A baseband processor according to claim 80 wherein said demodulator further comprises:
a first carrier tracking loop for the third format; and
a second carrier tracking loop for the first and second formats.

83. A baseband processor according to claim 82 wherein said second carrier tracking loop comprises:
a carrier numerically controlled oscillator (NCO); and
a controller to selectively operate said carrier NCO based upon a carrier phase of said first carrier tracking loop to thereby facilitate switching to the format of the variable data.

84. A baseband processor according to claim 82 wherein said second carrier tracking loop comprises:
a carrier loop filter; and
a controller to selectively operating said carrier loop filter based upon a frequency of said first carrier tracking loop to thereby facilitate switching to the format of the variable data.

85. A baseband processor according to claim 78 wherein said modulator is further configured to partition data into four bit nibbles of sign (one bit) and magnitude (three bits) to said at least one predetermined orthogonal code function encoder.

86. A baseband processor according to claim 78 wherein the predetermined orthogonal code is a Walsh code modified by a modulo two addition of a fixed hexadecimal code thereto.

87. A baseband processor according to claim 78 wherein the predetermined orthogonal code is a bi-orthogonal code.

88. A baseband processor according to claim 78 wherein said at least one predetermined orthogonal code function correlator comprises:
a predetermined orthogonal code function generator; and
a plurality of parallel connected correlators connected to said predetermined orthogonal code function generator.

89. A baseband processor according to claim 78 wherein said modulator is configured to spread each data bit using a pseudorandom (PN) sequence at a predetermined chip rate and is configured to generate a preamble; and wherein said demodulator comprises preamble demodulator means for demodulating the preamble for achieving initial PN sequence synchronization.

90. A baseband processor according to claim 78 wherein said modulator comprises a scrambler; and wherein said demodulator comprises a descrambler.

91. A baseband processor for a spread spectrum radio transceiver, said baseband processor comprising:
a modulator for spread spectrum phase shift keying (PSK) modulating information for transmission, said modulator comprising
at least one encoder for encoding information for transmission,
wherein said modulator is configured to operate in one of a first format defined by bi-phase PSK (BPSK) modulation at a first data rate and a second format defined by quadrature PSK (QPSK) modulation at a second data rate, and
[header modulator means for modulating] wherein said modulator is configured to modulate data packets to include a header at a third format defined by a predetermined modulation at a third data rate and variable data in one of the first and second formats; and
a demodulator for spread spectrum PSK demodulating received information, said demodulator comprising
at least one correlator for decoding received information,
wherein said demodulator is configured to operate in one of the first and second formats,
wherein said demodulator is configured to demodulate data packets by demodulating the header at the third format and for switching to the respective one of the first and second formats of the variable data after the header,
a first carrier tracking loop for the third format, and
a second carrier tracking loop for the first and second formats.

92. A baseband processor according to claim 91 wherein the predetermined modulation of the third format is differential BPSK (DBPSK), and wherein the third data rate is lower than the first and second data rates.

93. A baseband processor according to claim 91 wherein said second carrier tracking loop comprises:
a carrier numerically controlled oscillator (NCO); and

a controller for selectively operating said carrier NCO based upon a carrier phase of said first carrier tracking loop to thereby facilitate switching to the format of the variable data.

94. A baseband processor according to claim 91 wherein said second carrier tracking loop comprises:
a carrier loop filter; and
a controller to selectively operate said carrier loop filter based upon a frequency of said first carrier tracking loop to thereby facilitate switching to the format of the variable data.

95. A baseband processor according to claim 91 wherein said modulator is configured to spread each data bit using a pseudorandom (PN) sequence at a predetermined chip rate and is further configured to generate a preamble; and wherein said demodulator is configured to demodulate the preamble for achieving initial PN sequence synchronization.

96. A baseband processor according to claim 91 wherein said modulator comprises a scrambler; and wherein said demodulator comprises a descrambler.

97. A modulator for a spread spectrum radio transceiver, said modulator configured to modulate information for transmission by spread spectrum phase shift keying (PSK), said modulator comprising at least one predetermined orthogonal code function encoder for encoding information according to a predetermined orthogonal code for reducing an average DC signal component.

98. A modulator according to claim 97 wherein said modulator is configured to operate in one of first format defined by bi-phase PSK (BPSK) modulation at a first data rate and a second format defined by quadrature PSK (QPSK) modulation at a second data rate.

99. A modulator according to claim 98 wherein said modulator is configured to modulate data packets to include a header at a third format defined by a predetermined modulation at a third data rate and variable data in one of the first and second formats.

100. A modulator according to claim 99 wherein the predetermined modulation of the third format is differential BPSK (DBPSK), and wherein the third data rate is lower than the first and second data rates.

101. A modulator according to claim 97 wherein said modulator is configured to partition data into four bit nibbles of sign (one bit) and magnitude (three bits) to said at least one predetermined orthogonal code function encoder, and wherein the predetermined orthogonal code is a Walsh code modified by a modulo two addition of a fixed hexadecimal code thereto.

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102. A modulator according to claim 97 wherein said at least one predetermined orthogonal code function correlator comprises:
a predetermined orthogonal code function generator; and
a plurality of parallel connected correlators connected to said predetermined orthogonal code function generator.

103. A modulator according to claim 97 wherein the predetermined orthogonal code is a Walsh code modified by a modulo two addition of a fixed hexadecimal code thereto.

104. A modulator according to claim 97 wherein the predetermined orthogonal code is a bi-orthogonal code.

105. A demodulator for a spread spectrum radio transceiver, said demodulator configured to demodulate information for by spread spectrum phase shift keying (PSK) said demodulator for spread spectrum phase shift keying (PSK) demodulating information received from a radio circuit, said demodulator means comprising at least one predetermined orthogonal code function correlator for decoding information according to a predetermined orthogonal code reducing an average DC signal component.

106. A demodulator according to claim 105 wherein said demodulator is configured to operate in one of first format defined by bi-phase PSK (BPSK) modulation at a first data rate and a second format defined by quadrature PSK (QPSK) modulation at a second data rate.

107. A demodulator according to claim 106 wherein said demodulator is configured to demodulate data packets including a header in a third format defined by a predetermined modulation at a third data rate and variable data in one of the first and second formats, and for switching to the respective one of the first and second formats of the variable data after the header.

108. A demodulator according to claim 107 wherein the predetermined modulation of the third format is differential BPSK (DBPSK), and wherein the third data rate is lower than the first and second data rates.

109. A demodulator according to claim 107 wherein said demodulator further comprises:
a first carrier tracking loop for the third format; and
a second carrier tracking loop for the first and second formats.

110. A demodulator according to claim 109 wherein said second carrier tracking loop comprises:
a carrier numerically controlled oscillator (NCO); and
a controller to selectively operate said carrier NCO based upon a carrier phase of said first carrier tracking loop to thereby facilitate switching to the format of the variable data.

111. A demodulator according to claim 109 wherein said second carrier tracking loop comprises:

a carrier loop filter; and

a controller to selectively operate said carrier loop filter based upon a frequency of said first carrier tracking loop to thereby facilitate switching to the format of the variable data.

112. A demodulator according to claim 105 further configured to partition data into four bit nibbles of sign (one bit) and magnitude (three bits).

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113. A demodulator according to claim 105 wherein the predetermined orthogonal code is a Walsh code modified by a modulo two addition of a fixed hexadecimal code thereto.

114. A demodulator according to claim 105 wherein the predetermined orthogonal code is a bi-orthogonal code.

115. A demodulator according to claim 105 wherein said at least one predetermined orthogonal code function correlator comprises:

a predetermined orthogonal code function generator; and

a plurality of parallel connected correlators connected to said predetermined orthogonal code function generator.

116. A method for baseband processor for spread spectrum radio communication, the method comprising:

spread spectrum phase shift keying (PSK) modulating information for transmission while encoding the information according to the predetermined orthogonal code for reducing an average DC signal component; and

spread spectrum PSK demodulating received information by decoding the received information according to the predetermined orthogonal code.

117. A method according to claim 116 further comprising AC-coupling received information for spread spectrum PSK demodulating so that the reduced average DC signal component in combination with the AC-coupling enhances overall performance.

118. A method according to claim 116 further comprising modulating and demodulating in one of first format defined by bi-phase PSK (BPSK) modulation at a first data rate and a second format defined by quadrature PSK (QPSK) modulation at a second data rate.

119. A method according to claim 118 further comprising:
modulating data packets to include a header at a third format defined by a predetermined modulation at a third data rate and variable data in one of the first and second formats; and
demodulating data packets by demodulating the header at the third format and for switching to the respective one of the first and second formats of the variable data after the header.

120. A method according to claim 119 wherein the predetermined modulation of the third format is differential BPSK (DBPSK), and wherein the third data rate is lower than the first and second data rates.

121. A method according to claim 116 wherein the predetermined orthogonal code is a Walsh code modified by a modulo two addition of a fixed hexadecimal code thereto.

122. A method according to claim 116 wherein the predetermined orthogonal code is a bi-orthogonal code.